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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,458	08/31/2000	David Golden	15311-2284	3570

24267 7590 12/19/2003

CESARI AND MCKENNA, LLP
88 BLACK FALCON AVENUE
BOSTON, MA 02210

EXAMINER	
NGUYEN, DUSTIN	
ART UNIT	**PAPER NUMBER**
2154	6

DATE MAILED: 12/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/652,458	GOLDEN ET AL.	
	Examiner	Art Unit	
	Dustin Nguyen	2154	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1 - 10 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4-6, 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins et al. [US Patent No 5,963,745], in view of Wilkinson et al. [US Patent No 5,815,723].

4. As per claim 1, Collins discloses the invention substantially as claimed including a multiprocessor computer system having a plurality of processors interconnected so that they can share memory, comprising:

a plurality of links [Figure 10], each link of said plurality of links connecting a processor to another processor [col 5, lines 45-56];

a router box (RBOX) associated with each processor of said plurality of processors [col 14, lines 65-67], said RBOX arranged to forward a message received on an input link of said plurality of links from a source processor to an outgoing link of said plurality of links toward a destination processor in response to data carried in said message [col 7, lines 40-50; and col 14, lines 44-56];

a plurality of microprocessors, each of said microprocessors having a microprocessor memory associated therewith [col 7, lines 8-37], a selected microprocessor of said plurality of microprocessors associated with at least one processor of said plurality of processors [col 15, lines 60-62], said plurality of microprocessors arranged to control said plurality of processors [Figure 18; and col 3, lines 65-col 4, lines 24], said control including applying electric power to a selected processor and removing electric power from said selected processor [col 42, lines 52-57];

Collins does not specifically disclose

a data structure stored in microprocessor memory, said data structure storing a representation of the links connecting said processors and storing routes used by said RBOX in routing messages along said links, a copy of said data structure stored in microprocessor memory of each of said microprocessors; and,

a process to update said data structure in each said microprocessor memory in the event that a change occurs in a status of a component of said multiprocessor computer system.

Wilkinson discloses

a data structure stored in microprocessor memory, said data structure storing a representation of the links connecting said processors and storing routes used by said RBOX in routing messages along said links, a copy of said data structure stored in microprocessor memory of each of said microprocessors [Abstract; col 4, lines 19-24; and col 19, lines 3-8] ; and,

a process to update said data structure in each said microprocessor memory in the event that a change occurs in a status of a component of said multiprocessor computer system [col 31, lines 1-35].

It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Collins and Wilkinson because Wilkinson's teaching would allow configuration information to be updated to for the processors to prevent system failure.

5. As per claim 4, Collins discloses

an input/output (I0) subsystem associated with selected processors of said plurality of processors [col 7, lines 11-15];

an IO microprocessor associated with each said I0 subsystem [col 4, lines 6-12], said I0 microprocessor communicating with said microprocessors through said local area network [Figures 15 and 18], each said IO microprocessor having an I0 microprocessor memory holding a copy of said database [Figure 10; and col 73, lines 54-55];

a process executing in said I0 microprocessor, said process responsive to said database, said process to apply power or remove power to said I0 subsystem [col 42, lines 52-57].

6. As per claim 5, Collins discloses

a boot-up process executing in microprocessors of said plurality of microprocessors, said boot-up process to start execution of said processors of said multiprocessor system, and said multiprocessor system capable of continuing operation, after start of execution of said processors, to permit removal of a microprocessor from the multiprocessor system without interrupting execution of said processors [col 52, lines 33-35; and col 35, lines 1-5].

7. As per claims 6, 9, 10, they are method claimed of claims 1, 4, 5, they are rejected for similar reasons as stated above in claims 1, 4, 5.

8. Claims 2, 3, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins et al. [US Patent No 5,963,745], in view of Wilkinson et al. [US Patent No 5,815,723], and further in view of Wilkinson et al. [US Patent No 5,878,241].

9. As per claim 2, Collins and Wilkinson [US Patent No 5,815,723] do not specifically disclose

a process executing in said microprocessors for directing said microprocessors in formation of a partition of said processors, said partition having a selected number of said processors as members, said members capable of reading and writing a common memory within said partition, and other non-member processors excluded from reading and writing said common memory; and,

a second data structure for storing a representation of said partitions, and storing routes through said links for transfer of messages between processors within a partition but not between processors of different partitions.

Wilkinson [US Patent No 5,878,241] discloses

a process executing in said microprocessors for directing said microprocessors in formation of a partition of said processors, said partition having a selected number of said processors as members [col 71, lines 32-36], said members capable of reading and writing a

common memory within said partition, and other non-member processors excluded from reading and writing said common memory [col 25, lines 8-10]; and,

a second data structure for storing a representation of said partitions, and storing routes through said links for transfer of messages between processors within a partition but not between processors of different partitions [col 70, lines 57-col 72, lines 4; col 72, lines 55-58; and col 73, lines 4-8].

It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Collins, Wilkinson [US Patent No 5,815,723], and Wilkinson [US Patent No 5,878,241] because Wilkinson [US Patent No 5,878,241]'s teaching would allow tasks or processes to be broken into smaller portions and each can be handled by a group of processors for better system performance.

10. As per claim 3, Collins discloses

a management computer communicating through said local area network with said microprocessors, said management computer having an input device such as a keyboard and mouse for entering commands to said plurality of microprocessors to modify said data base in order to establish the processors belonging to a partition, said multiprocessor computer system supporting a plurality of said partitions [Figure 22; and col 52, lines 21-39];

a process responsive to said data base, said process executing in said microprocessors to establish that a processor in a partition can read and write memory associated with other processors of said partition, but cannot read and write memory associated with processors which are not members of said partition [col 25, lines 8-10].

11. As per claims 7, 8, they are method claimed of claims 2, 3, they are rejected for similar reasons as claimed 2, 3.

12. A shortened statutory period for response to this action is set to expire **3 (three) months and 0 (zero) days** from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 U.S.C 133, M.P.E.P 710.02, 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (703) 305-5321. The examiner can normally be reached on Monday – Friday (8:00 – 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (703) 305-9678.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directly to the receptionist whose telephone number is (703) 305-3900.

Dustin Nguyen

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100